IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant: Hajime NAKAYAMA

Old Attorney Docket No.: P98,2413
New Attorney Docket No.: 09792909-4043

Serial No.: 09/210,540 Art Unit: 2811

Filed: December 14, 1998 Examiner: D. Kang

For: **SEMICONDUCTOR DEVICE**

APPELLANT'S MAIN BRIEF ON APPEAL

Assistant Commissioner for Patents
Washington D.C. 20231

Sir:

Appellant is submitting herewith, in triplicate, Appellant's Main Brief on Appeal under 37 C.F.R. §1.192 in support of the Notice of Appeal filed on September 5, 2001.

The Commissioner is hereby authorized to charge any fee due not paid by check and to credit any overpayment in fees associated with this communication to Deposit Account No. 19-3140. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

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CERTIFICATE OF MAILING

I hereby certify that this original and two copies of this correspondence is being deposited with the United States Postal Service by First Class Mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231 on September 5, 2001.

Kathleen Gaines

Kathleen Gaines

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Hon. Assistant Commissioner for Patents
Washington D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. §1.192, Appellant herewith submits this Brief in support of the Appeal of the above-referenced application.

REAL PARTY IN INTEREST:

The real party in interest in the present appeal is the Assignee, Sony Corporation, a Japanese Corporation. The assignment was recorded in the U.S. Patent and Trademark Office on December 14, 1998 at Reel/Frame 9643/0989.

RELATED APPEALS AND INTERFERENCES:

There are no related appeals and no related interferences.

STATUS OF CLAIMS:

For purposes of appeal, claims 1 and 3-11 are pending in the application. Claims 1-11 were present in the original application. Claim 2 having been withdrawn from consideration. Appellant therefore appeals the final rejection of claims 1 and 3-11.

The status of the claims on appeal is as follows:

Claims 1, 3-5, and 9-11 are rejected as unpatentable under 35 U.S.C. 103(a) as being obvious over a combination of the prior art devices shown in Figures 1-3 of Appellant's application and United States Patent No. 5,856,215 (Jung).

Claims 6-8 stand rejected as unpatentable under 35 U.S.C. 103(a) as being obvious over a combination of the prior art devices shown in Figures 1-3 of Appellant's application, Jung, and United States Patent No. 6,114,741 (Joyner *et al.*).

STATUS OF AMENDMENTS:

Subsequent to the Final Office Action of March 5, 2001, Appellant filed on June 5, 2001 a proposed amendment under 37 C.F.R. § 1.116. The Examiner, in an Advisory Action dated June 26, 2001, acknowledged the cancellation of claim 2, and stated that the proposed amendment of claim 1 would be entered upon the timely submission of a Notice of Appeal and Appeal Brief.

SUMMARY OF THE INVENTION:

Appellant has discovered an improved semiconductor device having a pair of element formation regions separated by an element isolation region. (*United States Patent Application No. 09/210,540*, page 5, line 5 - page 6, line 4.) The device employs a pair of gate electrodes containing impurities of different conductivity types. (*Id.*) Connected to the gate electrodes are a pair of impurity storage regions arranged in a direction different from the direction of

the arrangement of the gate electrodes. (*Id.*) The impurity storage regions can be physically connected to each other by a semiconductor layer. (*Id.* at page 6, lines 5-7.) The semiconductor layer can be formed of polycrystalline silicon, and the gate electrodes and impurity storage regions can be formed by selectively implanting impurities to the polycrystalline silicon layer. (*Id.* at page 6, lines 8-12.) The width of the semiconductor layer can be a value allowing mask misalignment when forming the pair of gate electrodes and impurity storage regions. (*Id.* at page 6, lines 13-18.) The element isolation region can be buried in a trench formed of a boundary between the element formation regions. (*Id.* at page 7, lines 6-10.) The element isolation region can isolate the element formation regions comprised of semiconductor layers formed on an insulation layer. (*Id.* at page 7, lines 11-14.) The element isolation region can be buried in a trench formed in the semiconductor layers. (*Id.* at page 7, lines 15-16.) The widths of the impurity storage regions can be equal to the gate length of the gale electrodes and the lengths of the impurity storage regions can be longer than the gate length. (*Id.* at page 7, lines 17-21.)

ISSUES:

The issues on Appeal are as follows:

(1) whether claims 1, 3-5 and 9-11 are unpatentable under 35 U.S.C § 103(a) as being obvious over a combination of the prior art devices shown in Figures 1-3 of Appellant's application and United States Patent No. 5,856,215 (Jung); and

(2) whether claims 6-8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over a combination of the prior art devices shown by Applicant in Figures 1-3, Jung, and United States Patent No. 6,114,741 (Joyner *et al.*).

GROUPING OF CLAIMS:

For purposes of appeal, claims 1 and 3-11 stand or fall together.

ARGUMENT:

I. Claims 1, 3-5 and 9-11 Are Not Obvious

Claims 1, 3-5, and 9-11 are rejected as unpatentable under 35 U.S.C. § 103(a) as being obvious over a combination of the prior art devices shown in Figures 1-3 of Appellant's application and United States Patent No. 5,856,215 (Jung). However, the Examiner has not made the requisite showing that these claims are obvious in view of the cited art.

Figure 1 of Jung shows a semiconductor device having two element formation regions separated by an element isolation region. The semiconductor device contains a pair of L-shaped gate electrodes. As appreciated by the examiner, the electrodes are not physically connected by a semiconductor layer. Therefore there is no possibility of the impurities migrating into a semiconductor layer. *A fortiori*, Jung does not disclose or suggest a semiconductor device having first and second impurity storage regions, let alone a semiconductor device that includes a region that is effective for an impurity storage, while shortening the distance between the gate electrodes.

Instead, it appears that the legs of the first and second L-shaped gate electrodes 12 and 22, are incorporated to provide ample material to create a base for securing the metal wire 5C which connects the gate electrodes. As explained at column, lines 9-12, "the areas of the first gate electrode 12 and the second gate electrode 22 have to be large considering the contact margin, which limits the reduction of the size of the chip."

The Examiner urges that it would have been obvious to substitute the L-shaped electrode shown in Jung for the prior art electrode shown in Figure 2 of Appellant's application. However, the Examiner has the burden to show some teaching or suggestion *in*

the references to support their use in the particular claimed combination. *SmithKline Diagnostics Inc. v. Helena Laboratories Corp.*, 8 U.S.P.Q.2d 1468, 1475 (Fed. Cir. 1988). The absence of such a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 42 U.S.P.Q.2d 1378, 1383 (Fed. Cir. 1997). The references relied upon by the Examiner provide no such suggestion or motivation. Applicant respectfully submits that the Examiner's assertion, "It would have been obvious to one of ordinary skill to change shape of gate electrode (sic) in order to achieve high density of CMOS on a wafer," at least as it applies to Applicants' claimed configuration, is based on impermissible hindsight. To draw on hindsight knowledge of the patented invention, when the prior art does not contain or suggest that knowledge, is to use the invention as a template for its own reconstruction -- an illogical and inappropriate process by which to determine patentability. *Sensonics Inc. v. Aerosonic Corp.*, 38 U.S.P.Q.2d 1551, 1554 (Fed. Cir. 1996).

> In the Advisory Action dated June 26, 2001, the Examiner states:
>
> Jung teaches that the first and second gate electrode portions (12' & 22') connected to an end of gate electrodes (12 & 22) (sic) and arranged in a direction different from the direction of arrangement of first and second gate electrodes. This arrangement of impurity doped region *shortens* the distance between NMOS and PMOS and further reduces the chip area.

Paper No. 9, pages 2-3 (emphasis added).

On the contrary, the arrangement does not inherently shorten the distance between the NMOS and PMOS. This arrangement is designed to provide added material to facilitate the metal wiring that creates the connection between the gate electrodes. There is no suggestion that this added material in any way shortens the distance between the two. In fact, it is more likely that the material is added at the expense of increasing the distance between the NMOS and PMOS. For the above reasons, the Examiner has not made the requisite showing that claims 1, 3-5, and 9-11 are unpatentable under 35 U.S.C. 103(a) as being obvious over the cited art.

II. Claims 6-8 Are Not Obvious

Claims 6-8 are rejected as unpatentable under 35 U.S.C. 103(a) as being obvious over a combination of the prior art devices shown in Figures 1-3 of Appellant's application, Jung, and further in view of United States Patent No. 6,114,741 (Joyner *et al.*). However, the Examiner has not made the requisite showing that these claims are obvious in view of the cited art.

The Examiner has cited Joyner *et al.* merely because it teaches an element isolation region buried in a trench formed at a boundary between the element formation regions. However, nothing in any of these references whether considered alone or considered together would have suggested a semiconductor device having a pair of impurity storage regions physically connected by a semiconductor layer and arranged in a direction different from the direction of the arrangement of the gate electrodes. For the above reasons, the Examiner has not made the requisite showing that claims 6-8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the cited art.

CONCLUSION:

In summary, Appellant submits that the Examiner has failed to make the requisite showing that claims 1 and 3-11 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the cited art, and therefore earnestly solicits reversal of the decision of the Examiner to reject claims 1 and 3-11. Appellant solicits allowance of all claims.

Respectfully submitted,

Date: September 5, 2001

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APPENDIX

1. A semiconductor device comprising:

a first element formation region in which a device of a first conductivity type is formed;

a second element formation region separated from said first element formation region by an element isolation region and in which a device of a second conductivity type different from said first conductivity type is formed;

a first gate electrode provided on said first element formation region and containing an impurity of the first conductivity type;

a second gate electrode provided on said second element formation region facing said first gate electrode and containing an impurity of the second conductivity type;

a first impurity storage region containing said first conductivity type impurity, having one end connected to an end of said first gate electrode, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes; and

a second impurity storage region, physically connected to said first impurity storage region by a semiconductor layer, said second impurity storage region containing said second conductivity type impurity, and having one end connected to an end of said second gate electrode, having the other end electrically connected to the other end of said first impurity storage region, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes.

3. A semiconductor device as set forth in claim 1, wherein the other ends of said first and second impurity storage regions are electrically connected to each other through a conductive layer.

4. A semiconductor device as set forth in claim 1, wherein said first and second impurity storage regions are arranged in a direction perpendicular to the direction of arrangement of said first and second gate electrodes.

5. A semiconductor device as set forth in claim 1, wherein said first and second gate electrodes and said first and second impurity storage regions are formed in the same conductive semiconductor layer.

6. A semiconductor device as set forth in claim 1, wherein said element isolation region is buried in a trench formed a boundary between said first and second conductive type of element formation regions in a semiconductor substrate.

7. A semiconductor device as set forth in claim 1, wherein said element isolation region isolates first and second element formation regions comprised of semiconductor layers formed on an insulation layer.

8. A semiconductor device as set forth in claim 7, wherein said element isolation region is buried in a trench formed in said semiconductor layers.

9. A semiconductor device as set forth in claim 2, wherein:

said semiconductor layer is formed by polycrystalline silicon and said first and second gate electrodes and first and second impurity storage regions are formed by selectively implanting impurities to said polycrystalline silicon layer.

10. A semiconductor device as set forth in claim 2, wherein the width of said semiconductor layer physically connecting said first and second impurity storage regions is a value allowing mask misalignment when forming said first and second gate electrodes and first and second impurity storage regions.

11. A semiconductor device as set forth in claim 1, wherein:

the widths of said first and second impurity storage regions are equal to the gate length of said first and second gate electrodes and the lengths of said first and second impurity storage regions are longer than said gate length.